Available online at http://www.journalijdr.com

ISSN: 2230-9926

IJDR

International Journal of
DEVELOPMENT RESEARCH

International Journal of Development Research
Vol. 4, Issue, 3, pp. 575-581, March, 2014

Full Length Research Article

IMPLEMENTATION OF dSPACE BASED NEW HYBRID PWM STRATEGIES FOR SINGLE PHASE SEVEN LEVEL CASCADED ASYMMETRICAL INVERTER

***[1]Johnson Uthayakumar. R., [2]Natarajan S. P. and [3]Shanthi, B.**

[1]Department of Electronics and Instrumentation, Research Scholar, Annamalai University, India
[2]Department of Electronics and Instrumentation, Annamalai University, India
[3]Central Instrumentation Services Laboratory, Annamalai University, India

ARTICLE INFO

Article History:

Received 08th January, 2014
Received in revised form
11th February, 2014
Accepted 15th February, 2014
Published online 14th March, 2014

Key words:

PD, POD, APOD,
COPWM,
VFPWM,
CONTROL DESK,
dSPACE, THD, V_{rms}

ABSTRACT

Multi Carrier Based Pulse Width Modulation (MCBPWM) technique have been used widely for switching of multilevel inverters due to simplicity and reduced computational requirements than the Space Vector Modulation (SVM). New hybrid MCBPWM techniques for the chosen single phase Asymmetrical Multi Level Inverter (AMLI) with Trapezoidal Amalgamated Reference (TAR) are proposed in this paper. The proposed Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD) and Carrier Overlapping (CO) Pulse Width Modulation (PWM) strategies are developed with triangular carrier above zero axis and rectified sine carrier below zero axis. The triggering pulses are generated using the dSPACE dS1103 hardware and front end tool control desk with MATLAB/SIMULINK/Real Time Interface (RTI) environment. The performance indices used are Total Harmonic Distortion (THD), Form factor (FF), Distortion factor (DF) and Root Mean Square (RMS) value of output voltage. It is observed that COPWM provides relatively better DC bus utilization and creates relatively lesser distortion for modulation index ma=0.7-1.

INTRODUCTION

Multi Level Inverters (MLI) are classified into three types: the flying capacitor inverter, the diode clamped inverter and the modular H-bridge inverter. In this work, modular H-bridge inverter is used. Tolbert *et al.* (2003) have derived a procedure to find all sets of switching angles for which the fundamental is produced while the 5th and 7th are eliminated. Palanivel and Dash (2010) have developed various carrier based pulse width modulation techniques which can minimise the total harmonic distortion and enhance the output voltage for a five level inverter. Du *et al.* (2009) discussed about the control of seven-level Hybrid Cascaded Multi Level Inverter (HCMLI) with fundamental frequency switching control and explained how its modulation index (m_a) range can be extended using triplen harmonic compensation. Seyezhai and Mathur (2007) have reduced the switching losses and improved the power quality in AMLI using variable frequency inverted sine PWM strategy. Chandra and Kumar (2006) presented an automatic switching pattern generation for multilevel cascaded H-Bridge inverters with equal DC voltage sources based on the Space Vector Pulse Width Modulation (SVPWM) technique. Jeevananthan *et al.* (2007) have proposed an Inverted Sine Carrier PWM (ISCPWM) method which used the conventional sinusoidal reference signal and an inverted sine carrier to produce better spectral quality and a higher fundamental component compared to the conventional Sinusoidal PWM (SPWM) without any pulse dropping. A survey of topologies, controls and applications of MLIs has been carried out by Rodriguez *et al.* (2002). Taleb *et al.* (2009) have proposed a neural implementation of a Harmonic Elimination Strategy (HES) to control a Uniform Step Asymmetrical Multilevel Inverter (USAMI). Chunmei Feng and Agelidis (2002) have used the Neutral Point Clamped (NPC) topology for evaluation of THD using multicarrier PWM schemes. McGrath and Holmes (2002) have presented a similar equivalence between the Phase Disposition (PD) carrier and space vector modulation strategies applied to diode clamped, cascaded N-level or hybrid multilevel inverters. Ben-brahim *et al.* (2003) have proposed that the fluctuations of the neutral-point voltage are also reduced using this switch pattern method. Nami *et al.* (2012) have optimized asymmetrical arrangement compared with a conventional four level inverter and found that it exhibits lesser switching losses and lesser harmonics. Seyezhai

Corresponding author: Johnson Uthayakumar, R.
Department of Electronics and Electronics Engineering, Research Scholar Annamalai University, India.

and Mathur (2012, 2010) have done a comparative evaluation between hybrid modulation strategy and the conventional phase disposition PWM method in terms of output voltage quality, power circuitry complexity, Distortion Factor (DF) and THD. Wang Shu Zheng *et al.* (2011) have proposed a three phase cascaded multilevel inverter for grid controled photo voltaic system.This paper presents harware realization of new PWM steategies for chosen asymmetrical seven level inverters. A seven level output voltage is achieved with two bridges in asymmetrical inverter whereas only five level output voltage will be achieved with two bridges in case of conventional cascaded MLI. In AMLI with lesser number switches more voltage levels can be achieved. Fig.1 shows the chosen asymmetrical single phase inverter. Each bridge has two pairs of complementary switches A_a and A_b and A_c and A_d. There are two bridges used in the single phase inverter. Fig.2 shows a sample SIMULINK/MATLAB model developed for multicarrier PWM strategy of an asymmetrical seven level single phase inverter. Fig.3 shows triggering pulses generated using MATLAB-SIMULINK/dSPACE for bipolar COPWM technique of the chosen inverter.

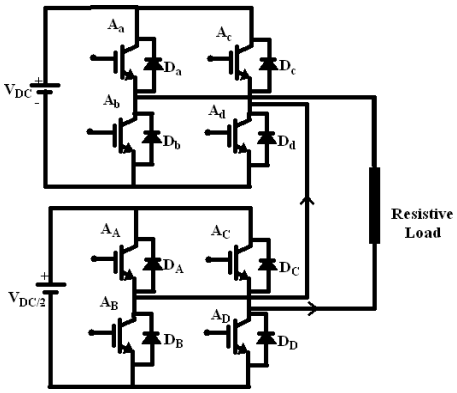

Fig.1 A single phase asymmetrical cascaded seven level inverter

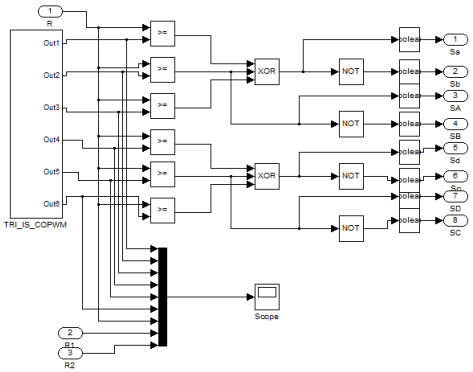

Fig.2. Sample PWM generation logic developed using MATLAB-SIMULINK for bipolar COPWM technique

Multilevel inverter

The term multilevel inverters began with the three level inverters. Several multilevel inverter topologies have been developed since 1975. The elementary concept of multilevel inverter is to achieve higher power and to use a series of power semiconductor switches with several lower voltage DC sources to perform the power conversion.

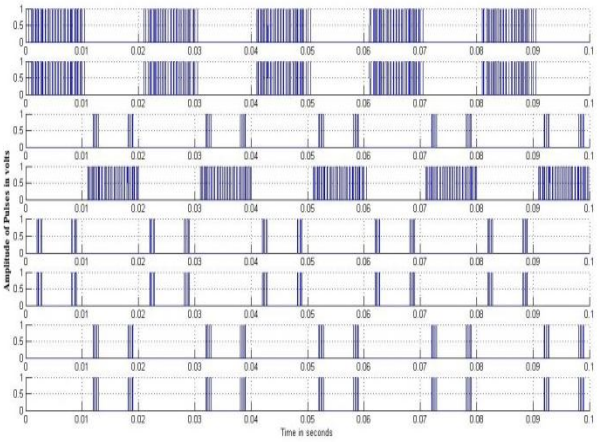

Fig.3. Triggering pulses generated using MATLAB-SIMULINK/dSPACE for bipolar COPWM technique

The general structure of multilevel inverters is to synthesize a near sinusoidal voltage from several DC voltages sources. Multilevel inverters offer several advantages. These include higher DC bus utilization, lesser switching losses, lower Total Harmonic Distortion (THD) and reduced switching stress in the power semiconductor switches. The proposed topology is single phase seven level asymmetrical multilevel inverter. The gating signals of the chosen single phase asymmetrical multilevel inverter are simulated and implemented using MATLAB/SIMULINK–dSPACE DS1103 controller. The proposed single phase seven AMLI uses two inverter bridges.The relation between number of inverter bridges (M) and output voltage levels (m) is

$$M = \frac{(m-3)}{2}$$

m=7 in this work and hence M=2
To find the amplitude modulation index m_a for the PD, POD, APOD, VF PWM multicarrier strategies the following equation is used:

$$m_a = \frac{2A_m}{(m-1)A_c}$$

A_c=Amplitude of carrier
A_m=Amplitude of the modulating signal (TAR)
A_m= 3Volts , A_c=1 Volt when m_a=1
To find the modulation index for the multicarrier strategy COPWM, the following equation is used.

$$m_a = \frac{A_m}{\left(\frac{m}{4}\right)A_c}$$

A_m= 2.8 Volts , A_c=1.6 Volt when m_a=1 in COPWM
To find the frequency modulation index m_f for all the modulation strategies, the following equation is used.

$$m_f = \frac{f_c}{f_m}$$

f_c=Frequency of the carrier signal
f_m=Frequency of the modulating signal
f_c= 4000Hz and f_m= 50Hz in this work and hence then m_f= 40

Modulation strategies

Since the multicarrier based PWM techniques have good Control Freedom Degree (CFD), this paper focusses on new hybrid carriers arrangements using triangular carrier in the positive side and rectified sine carrier waveform in the negative side with Phase Disposition (PD), Phase Opposition Disposition (POD), Alternate Phase Opposition Disposition (APOD), Carrier Overlapping (CO) and Variable Frequency (VF) PWM strategies. The modulating voltage is Trapizoidal Amalgamated Reference (TAR) reference signal. Fig.4 shows the arrangement for hybrid carrier PDPWM strategy with TAR reference for m_a=0.8 and m_f=40. Fig.5 displays the corresponding arrangement for PODPWM strategy. The arrangement for hybrid carrier APODPWM strategy with TAR reference is shown in Fig.6. Arrangement for hybrid carrier VFPWM strategy is displayed in Fig.7. Fig.8 shows the arrangement for hybrid carrier COPWM strategy with TAR reference.

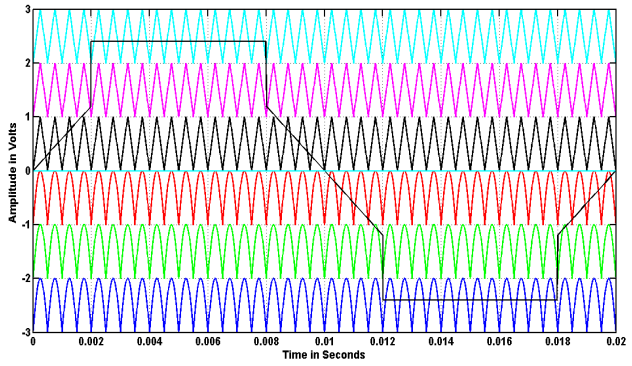

Fig.4. Arrangement for hybrid carrier PDPWM strategy with TAR reference (m_a=0.8 and m_f=40)

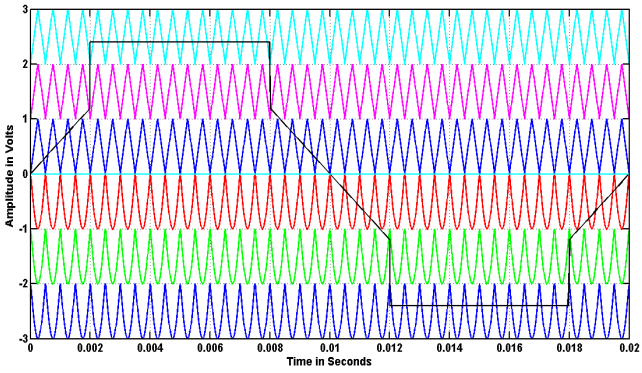

Fig.5. Arrangement for hybrid carrier PODPWM strategy with TAR reference (m_a=0.8 and m_f=40)

dSPACE EXPERIMENTAL SETUP

Fig.9 shows the experimental setup of the single phase seven level asymmetrical inverter interfaced with dSPACE. The entire setup can be divided into four modules: the control desk, the dSPACE interface module, the prototype of the single phase seven level asymmetrical multilevel inverter and the DC power supply with dual output for the input of the inverter.

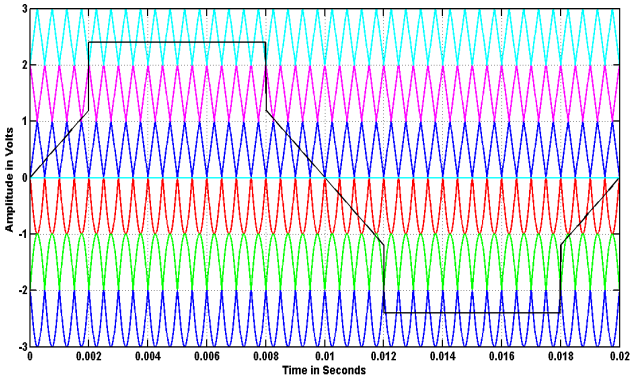

Fig.6. Arrangement for hybrid carrier APODPWM strategy with TAR reference (m_a=0.8 and m_f=40)

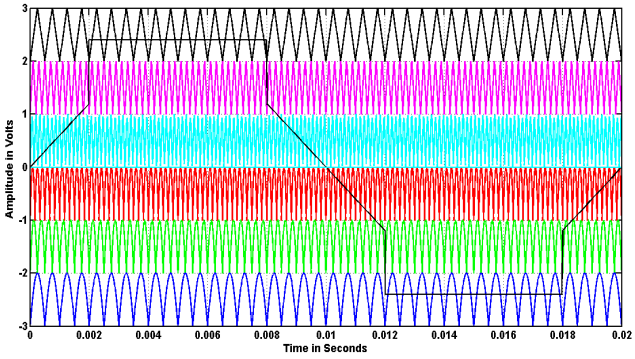

Fig.7. Arrangement for hybrid carrier VFPWM strategy with TAR reference (m_a=0.8 and m_f=40)

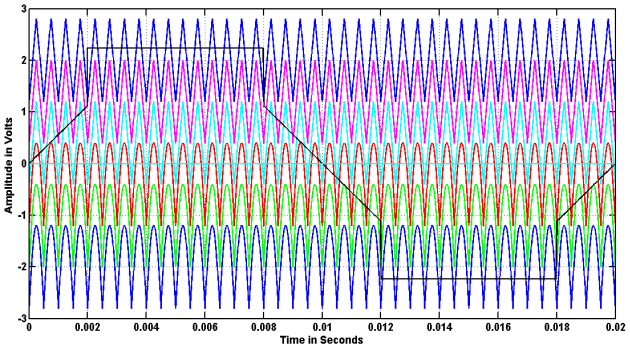

Fig.8 Arrangement for hybrid carrier COPWM strategy with TAR reference (m_a=0.8 and m_f=40)

dSPACE DS1103 controller board is based on the Texas Instruments TMS320F240 floating-point DSP. Real time implementation of the multicarrier PWM strategies using MATLAB – dSPACE/RTI requires less time for development as it can be expanded from the simulation blocks developed using MATLAB/ SIMULINK. The dSPACE system is an embedded or self-contained system. The dSPACE system combines a data acquisition system with an independent processing system to implement digital control. It is specifically designed for the development of high-speed multivariable digital controllers. The gate signal generation block using different PWM strategies listed above is designed and developed using SIMULINK and downloaded to dSPACE / RTI using control desk. Experimental tests are

carried out to validate the proposed ideas. The DS1103 card is plugged in one of the ISA slots of the mother-board of the host computer. The control circuit has been developed using MATLAB/SIMULINK and then automatically processed and run in the DS1103 card.

A Graphical User Interface (GUI) has been built using the software control desk for varying the amplitude modulation index using dSPACE/RTI. "control desk" serves multiple uses. The control desk is the software which is installed in the Personal Computer (PC) which enables the user to generate gating pulses required for the operation of the power switches in real time with the MATLAB/ SIMULINK/RTI environment. It provides the interface for downloading controller models designed in SIMULINK onto the DSP. The instrument panel feature of control desk is used to display various measurements such as the modulation index of the PWM signal. The amplitude modulation index is varied in real time and the readings are taken for m_a=0.7 -1. Signals must be sent through the "CLP1103" to "DS1103" The prototype of single phase seven level asymmetrical cascaded H-bridge inverter is constructed. Each of the two H-bridges has its own 10V and 5V DC power supplied from a regulated independent source. The MOSFET IRF840 is selected as inverter switch operating at 4000 Hz. The gating pulses to the H-Bridge inverters are generated by the dSPACE DS1103 controller. The gating pulses are further isolated by opto coupler 6N137 and an high and low side gate driver Integrated Circuit (IC) IR2110 for each pair of the MOSFET used. Transistor SL100 and 2N2222 act as additional driver for the MOSFETs.

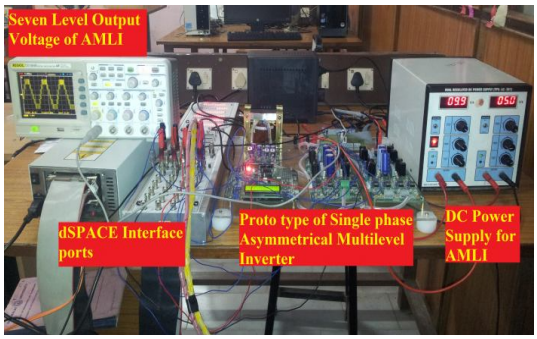

Fig.9. Experimental setup of single phase seven level asymmetrical cascaded multilevel inverter

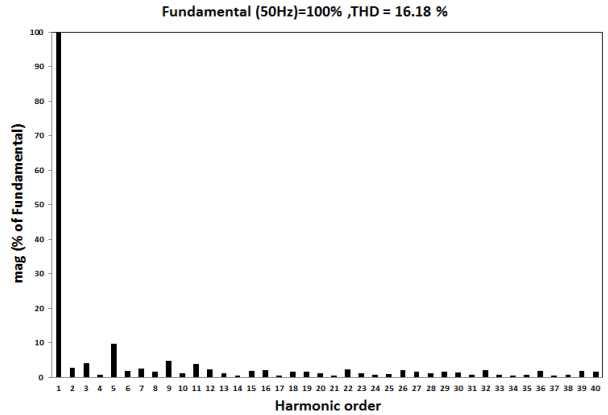

Fig.10. Practical FFT spectrum for hybrid PDPWM strategy for m_a=0.8 and m_f =40 with TAR reference

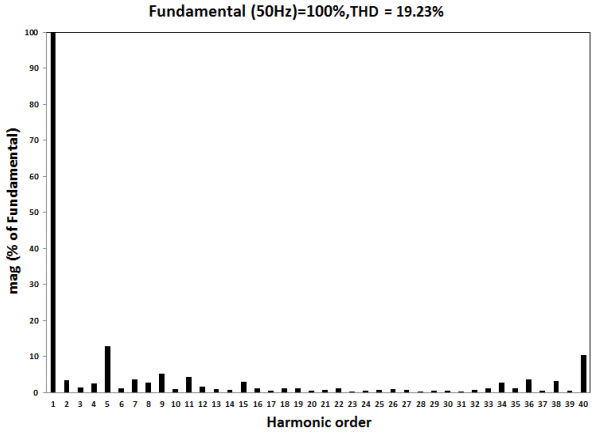

Fig.11. Practical FFT spectrum for hybrid PODPWM strategy for m_a=0.8 and m_f =40 with TAR reference

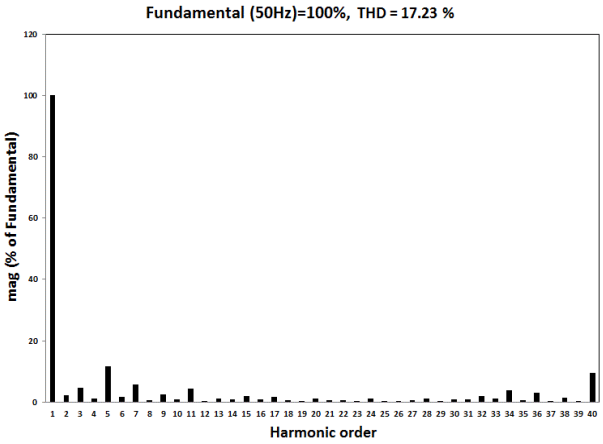

Fig.12. Practical FFT spectrum for hybrid APODPWM strategy for m_a=0.8 and m_f =40 with TAR reference

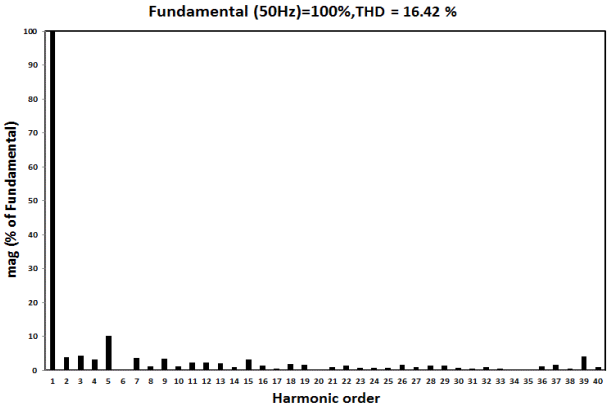

Fig.13. Practical FFT spectrum for hybrid VFPWM strategy for m_a=0.8 and m_f =40 with TAR reference

EXPERIMENTAL RESULTS

Inverter output voltages with various PWM stratergies and corresponding FFT plot are shown in Figs.15-19. From Fig.10 it is noticed that PDPWM strategy produces 5^{th}, 9^{th} and 13^{th} harmonic energy. From Fig.11, it is observed that PODPWM strategy produces 2^{nd}, 5^{th}, 7^{th}, 9^{th} ,11^{th} and 40^{th} harmonic energy.

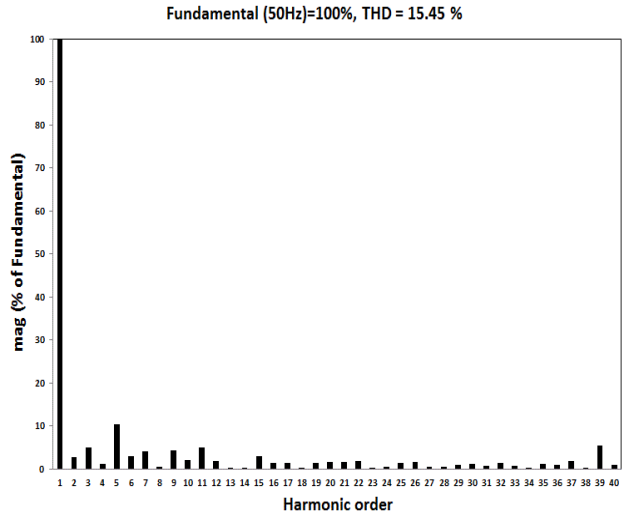

Fig.14. Practical FFT spectrum for hybrid COPWM strategy for m_a=0.8 and m_f =40 with TAR reference

From Fig.12 it is found that APODPWM strategy produces 3^{rd},5^{th},7^{th},11^{th},37^{th} and 40^{th} harmonic energy. Fig.13 shows that VFPWM produces 3^{rd},5^{th},7^{th},9^{th},11^{th} and 39^{th} harmonic energy. From Fig.14 it is observed that COPWM stratergy produces 2^{nd},3^{rd},4^{th},5^{th},7^{th},9^{th},13^{th} and 39^{th} harmonic energy. Table II shows the V_{rms} value of output voltage for m_a=0.7-1 and for all the chosen strategies as compared in Fig.20. It is found that the COPWM strategy provides relatively higher RMS output voltage. Table I indicates the THD values for m_a=0.7-1 and for all strategies as compared in Fig.21. It is again observed that COPWM creates relatively lower THD than other strategies. Table III displays the FF for m_a=0.7-1 and for all strategies as compared in Fig.23. Table V shows the DF for m_a=0.7-1 and for all strategies as compared in Fig.22. CF is tabulated in Table V

The following parameter values are used for experimentation: V_{dc1}=10V, V_{dc2}=5V, R(load)= 100Ω, f_c=4000 Hz, f_m=50 Hz, m_f=40.

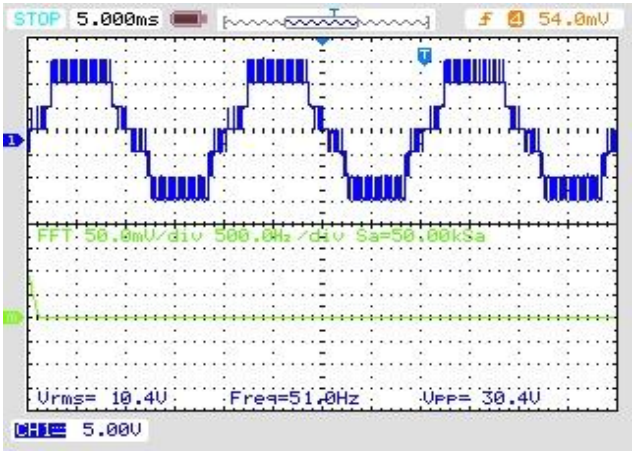

Fig.15. Output voltage of hybrid carrier PDPWM strategy with TAR reference

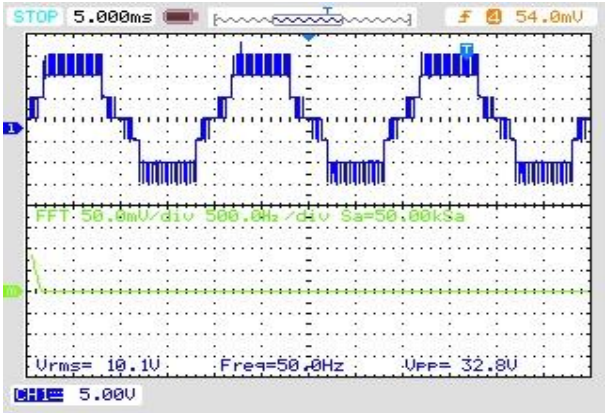

Fig.16. Output voltage of hybrid carrier PODPWM strategy with TAR reference

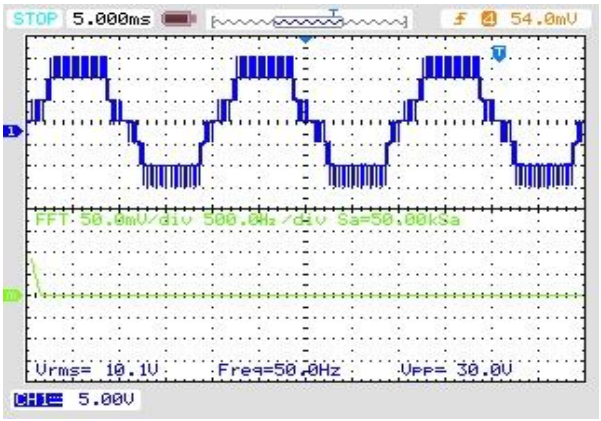

Fig.17. Output voltage of hybrid carrier APODPWM strategy with TAR reference

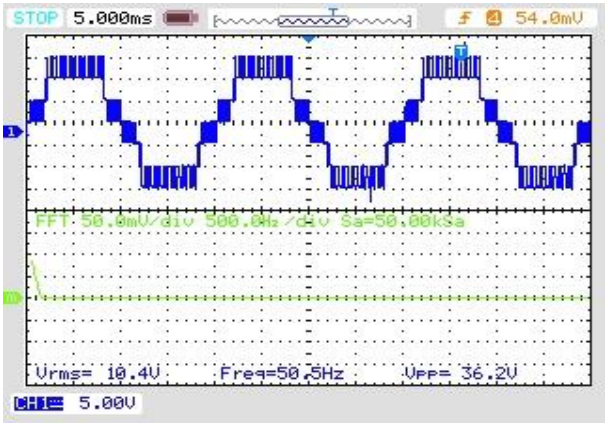

Fig.18. Output voltage of hybrid carrier VFPWM strategy with TAR reference

Table I. THD of the output voltage of AMLI for different PWM strategies and various values of m_a with TAR reference

m_a	PD	POD	APOD	VF	COPWM
1	15.72	19.26	16.65	15.50	16.47
0.95	16.18	19.23	17.23	15.45	16.42
0.9	15.77	20.75	17.23	16.10	15.47
0.85	14.96	20.30	18.99	17.09	16.02
0.8	15.29	20.35	18.80	17.16	15.62
0.75	17.38	19.61	19.50	17.34	15.32
0.7	17.79	19.93	20.08	17.33	15.24

Table II. V_{rms} of the output voltage of AMLI for different PWM strategies and various values of m_a with TAR reference

m_a	PD	POD	APOD	VF	COPWM
1	12.4	12.1	12.2	12.3	12.6
0.95	11.6	11.4	11.3	11.5	11.8
0.9	11.2	10.9	10.9	11.4	11.8
0.85	10.9	10.5	10.5	10.8	11.5
0.8	10.4	10.1	10.1	10.4	11.4
0.75	10.2	9.78	9.75	9.96	11.2
0.7	10.6	9.73	9.34	9.66	10.5

Table III. FF of the output voltage of AMLI for different PWM strategies and various values of m_a with TAR reference

m_a	PD	POD	APOD	VF	COPWM
1	1315	1227	1113	1651	1306
0.95	1620	1082	939	1148	1714
0.9	1328	978	962	1223	1294
0.85	1280	859	859	1310	1815
0.8	1195	957	875	1200	1622
0.75	1294	869	871	1242	1455
0.7	1224	893	852	1391	1274

Table IV. DF of the output voltage of AMLI for different PWM strategies and various values of m_a with TAR reference

m_a	PD	POD	APOD	VF	COPWM
1	0.0416	0.0406	0.0418	0.0420	0.0429
0.95	0.0403	0.0376	0.0386	0.0404	0.0416
0.9	0.0382	0.0354	0.0357	0.0387	0.0408
0.85	0.0362	0.0344	0.0345	0.0360	0.0393
0.8	0.0346	0.0318	0.0325	0.0348	0.0379
0.75	0.0326	0.0309	0.0309	0.0326	0.0367
0.7	0.0333	0.0292	0.0288	0.0308	0.0356

Table V. CF of the output voltage of AMLI for different PWM strategies and various values of m_a with TAR reference

m_a	PD	POD	APOD	VF	COPWM
1	1.110	1.110	1.110	1.110	1.110
0.95	1.110	1.110	1.110	1.110	1.110
0.9	1.110	1.110	1.110	1.110	1.110
0.85	1.110	1.110	1.110	1.110	1.110
0.8	1.110	1.110	1.110	1.110	1.110
0.75	1.110	1.110	1.110	1.110	1.110
0.7	1.110	1.110	1.110	1.110	1.110

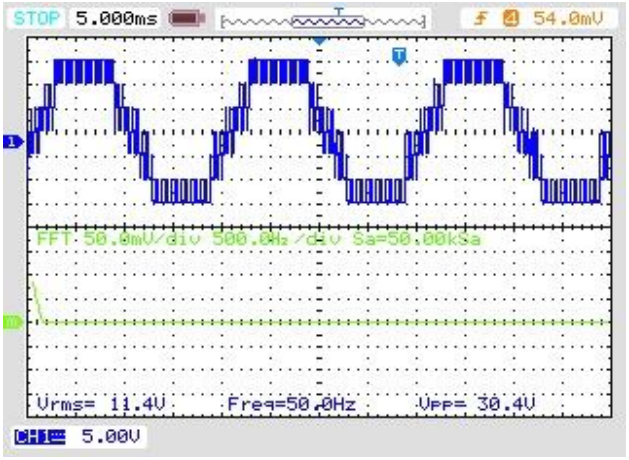

Fig.19. Output voltage of hybrid carrier COPWM strategy with TAR reference

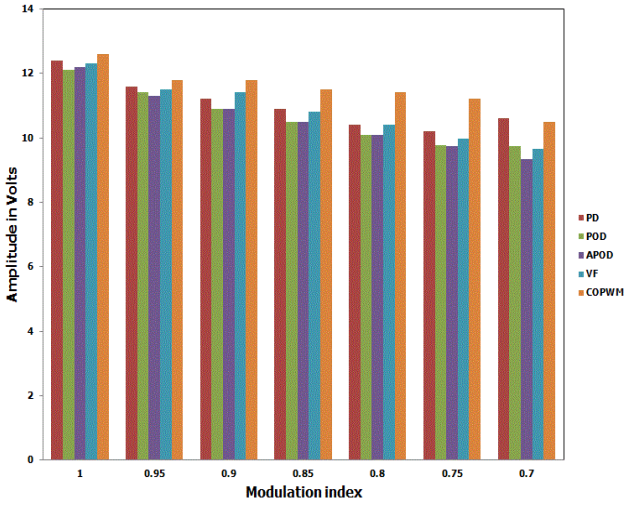

Fig.20 V_{rms} Vs. m_a

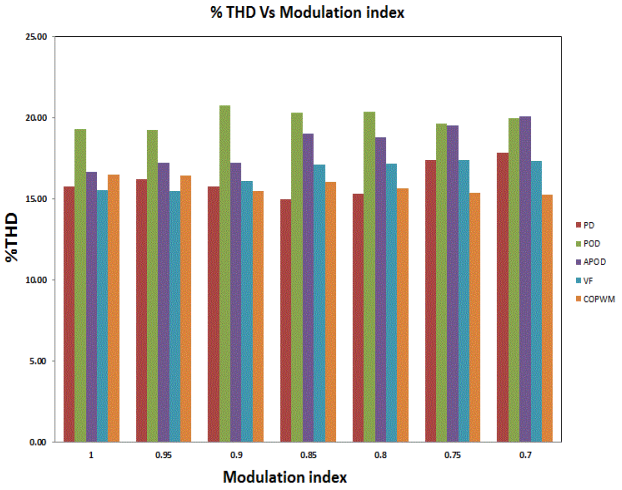

Fig.21.%THD Vs m_a

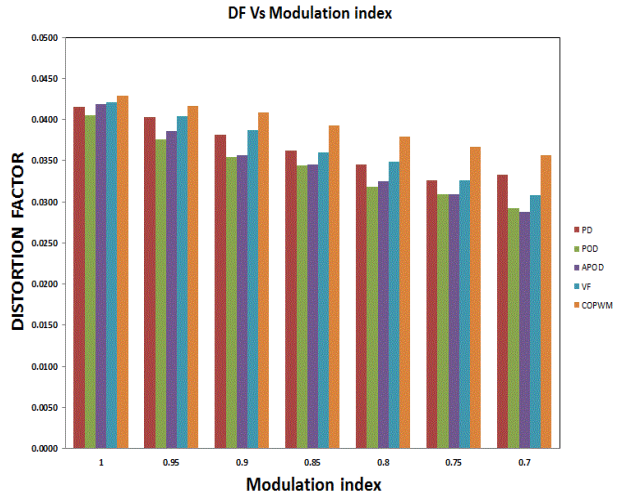

Fig.22. DF Vs. m_a

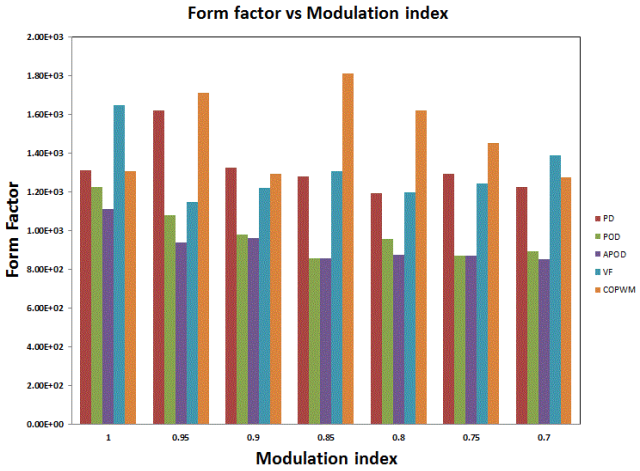

Fig.23 FF Vs. m_a

Conclusion

A prototype of a single phase seven level asymmetrical multilevel inverter has been developed in this work. New multicarrier hybrid PDPWM, PODPWM, APODPWM, VFPWM and COPWM strategies has been implemented in MATLAB/SIMULINK/dSPACE environment. The triggering pulses are developed for the power switches using dSPACE RTI. The modulation indicis are varied in the range of 0.7-1in real time using the control desk features in the MATLAB/SIMULNK/ dSPACE RTI. The performance indices such as the THD, V_{rms}, DF, FF and CF are calculated. It is observed that COPWM provides relatively better DC bus utilization and creates relatively lesser distortion for m_a=0.7-1. Experimental results presented using dSPACE/RTI validate the proposed PWM strategies.

REFERENCES

Ben-Brahim, L., Tadakuma, Susumu, "A new multilevel carrier-based PWM control method for GTO inverter in low index modulation region," *Industry Applications Conference, 2003. 38th IAS Annual Meeting. Conference Record of the*, vol.1, no., pp.664,671 vol.1, 12-16 Oct. 2003

Brendan Peter McGrath and Donald Grahame Holmes, "Sinusoidal PWM of Multilevel Inverters in the Over modulation Region", 33rd Annual Power Electronics Specialists Conference, june 2002.

Chandra K., J.Kumar, A. Simple and Generalized Space Vector PWM Control of Cascaded H-Bridge Multilevel Inverters. IEEE International Conference on Industrial Technology(ICIT), December 2006.

Chunmei Feng and G.Vassilios Agelidis, "On the Comparison of Fundamental and High Frequency Carrier-Based PWM Techniques for Multilevel NPC Inverters",33rd Annual Power Electronics Specialists Conference, june 2002.

Du Z., L. M. Tolbert, S. Member, B. Ozpineci, and J. N. Chiasson,"Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter", IEEE Transactions on Power Electronics, vol. 24, no. 1, pp. 25-33 Jan. 2009.

Jeevananthan S., R. Nandhakumar and P. Dananjayan, "Inverted Sine Carrier for Fundamental Fortification in PWM Inverters and FPGA Based Implementations", *Serbian Journal of Electrical Engineering*, Vol. 4, No. 2., pp. 171-18, November 2007.

Nami A., "Comparison between Symmetrical and Asymmetrical Single Phase Multilevel Inverter with Diode-Clamped Topology" 39rd IEEE Annual Power Electronics Specialists Conference, ", pp. 2921-2926, June 2008.

Palanivel P. P. and S. S. Dash, 2010. "Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques", *IET Power Electronics Received on 31st*, vol. 4, no. pp. 951-958 September 2011.

Rodriguez J., J.S. Lai, and F.Z. Peng, "Multilevel Inverter: A Survey of Topologies, Controls and Applications", *IEEE Trans. on Industrial Electronics*, Vol. 49 No. 4 pp. 724-738 Augest 2002.

Seyezhai R. and B.L. Mathur "Investigation of Variable Frequency ISPWM Control Method for an Asymmetric Multilevel Inverter", International Journal of Electrical & Computer Sciences IJECS vol: 9 No: 10 pp. 55-64, 2007

Seyezhai R., "Investigation of Performance Parameters For Asymmetric Multilevel Inverter Using Hybrid Modulation Technique", *International Journal of Engineering Science and Technology (IJEST)*, vol.3,pp.8430-8443. 2012.

Seyezhai R., B.L. Mathur "Hybrid Multilevel Inverter using ISPWM Technique for Fuel Cell Applications", *International Journal of Computer Applications (0975 – 8887)* volume 9, No.1, November 2010.

Taleb R., A. Meroufel, Control Multilevel Inverter switching strategy for of Asymmetrical Using Artificial Neural Network, Journal -Electronics and Electrical Engineering, No. 8(96), pp. 93-98, 2009.

Tolbert L. M., J. Chiasson, K. Mckenzie, and Z. Du, 2005. "Elimination of Harmonics in a Multilevel Converter with Non Equal DC Sources", IEEE Transactions On Industry Applications, Vol. 41, No. 1, pp. 589-595, January/February 2003.

Wang Shu Zheng; Zhao Jian Feng and Shi Chao "Research on a Three-Phase Cascaded Inverter For Grid-Connected Photovoltaic Systems", *Conference on Advanced Power System Automation and Protection (APAP), 2011 International*, 16-20 vol.1, no., pp.543-548 Oct2011

****