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A HYBRID NEUTRAL POINT CLAMPED MULTILEVEL BOOST INVERTER TOPOLOGY

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ABSTRACT

Multilevel inverters (MLI) have been a suitable alternate to three level inverters in medium/high power applications due to reduced voltage distortion, lesser voltage stress, lower electromagnetic interference (EMI) and improved power quality. The MLI have the distinctive advantage of increased voltage level with reduced switching stress while it suffers from increased power components. In this paper, a new MLI is proposed to nurture the power component count while increasing the number of voltage levels. In this direction, a traditional dc-dc boost converter is tailored with three level neutral point clamped inverters to introduce asymmetric voltages in the dc-link bus capacitors thereby increased voltage levels in the output terminals. For simplicity, the operating modes of the proposed inverter are studied using Selective Harmonic Elimination (SHE) and the same is simulated in MATLAB platform. The pulse generation methodology acquired through Field Programmable Gate Array (FPGA) that used to elicit the gating signals for the proposed inverter and is validated with a laboratory prototype of 1KW. The simulation results accorded with the experimental results to facilitate the proposed inverter suitable for renewable energy applications.

INTRODUCTION

Multilevel inverters have been a potential candidate for high power and medium voltage applications due to lesser blocking voltage, low harmonic distortion and low $\frac{dv}{dt}$ (Nabae *et al*., 1981). There are three benchmark topologies namely Diode clamped or neutral point clamped (Nabae *et al*., 1981), Flying capacitor (Teodorescu *et al*., 1999) and cascaded multilevel inverter (Manjrekar and Venkataramanan, 1996; Lai and Peng, 1996; Rodriguez *et al*., 2002; Malinowski *et al*., 2010; Rodriguez *et al*., 2010; Bhagwat and Stefanovic, 1983; Peng *et al*., 1995; Zheng Peng, 2001; Tolbert *et al*., 1999). In particular, Diode clamped inverter is the most admired topology for renewable energy applications, but it employ excessive clamping diodes when the number of levels is high. To overcome these drawbacks, several attempts have been made to minimize the power components by introducing a minor modification in the basic topologies (Rodrı´guez *et al*., 2007; Franquelo *et al*., 2008; Bernet, 2004; Rodrı´guez *et al*., 2005; Franquelo *et al*., 2006; Zhong *et al*., 2006; Tolbert *et al*., 1999; Dixon and Moran, 2006; Song *et al*., 2009). Several attempts have been made to bring a new innovation in multilevel inverter and its control strategies (Carrara *et al*., 1990; Sinha and Lipo, 1997). In this way, Multi-output DC/DC converters have been adopted due to their feasibility in the power conversion mode (buck/boost operation) that incorporated with MLI topologies (Zhong *et al*., 2006; Meynard and Foch, 1992). Several dc-dc converter configurations require bulky transformers to supply the utility loads that leads size and cost of the total system is increased. Later, new arrival of multi-output DC/DC converter is constituted by single-inductor and few power components whose outputs can be connected in parallel or series (Ramkumar *et al*., 2012). Out of these configurations, series type dc- dc converters are capable of reducing the dependency of DC-link voltage balancing and power factor of the load. Diode clamped MLI cannot balance their upper DC-link capacitors when supplying higher power factor loads. Further, there is a chance to bring an advancement in the power quality of a MLI by charging the DC-link capacitors asymmetrically that facilitates the utilization of quality advantage of asymmetrically supplied DC-links. The modulation method adopted for multilevel inverter is quite challenging as it is derived from three level modulations. All carrier modulation strategies is derived from phase disposition techniques developed by Carrara *et al*, where for an ‘m’ level inverter, m-1 carriers of same frequency and constant magnitude that

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are arranged to occupy contiguous bands between +V, and –V (Carrara *et al*., 1990; Sinha and Lipo, 1997). These carriers can be disposed in three ways (i) Alternative Phase Opposition Disposition (APOD), where each carrier is phase shifted by 180^o from its adjacent carriers. (ii) Phase Opposition Disposition (POD), where the carriers above the reference zero point is out of phase with those below the zero point by 180^o. (iii) Phase Disposition (PD) where all carriers are in phase. These modulation schemes involve high frequency switching and poor utilization of dc-link voltages. Few decades back, PWM based on axis conversion that utilizes effective utilization of dc-link voltages and improved performance indices than conventional methods (Carrara *et al*., 1990; Sinha and Lipo, 1997). There is any way of controlling the output voltage and harmonic magnitude through SHE that involves fundamental switching and have lesser switching loss. Hence in this study, SHE is used to control the proposed inverter. This paper proposed a novel, generalized single-inductor multi-output DC-DC MLI topology. This configuration has the advantage of different voltage magnitude across the capacitor dividers thereby increasing the number of voltage levels at the output for the same number of devices used in conventional three level neutral point clamped inverter.

Proposed topology

A generalized circuit for multi-output dc-dc MLI topology is portrayed in Fig.1. The circuit is formulated by dividing the output of classical dc- dc converter to produce asymmetrical multi-output through clamping circuit and then integrated with diode clamped MLI. The proposed topology has the merit of charging the dc-link capacitors with unequal voltages. For simplicity, a seven level inverter is shown in Fig. 2. To explain the operation of proposed inverter, the analysis is performed in two sections, first one with multi-output dc-dc converter and later diode clamped inverter. Figs. 3 to 6 show the operating mode for charging and discharging behavior of the dc-link capacitors. Fig. 7 shows the timing diagram for operating modes of multi-output dc-dc converter. To illustrate the charging/discharging behavior of dc-link capacitors, the period 'T' can be divided into three sub-intervals, where 'T' is the switching period of dc-dc converter. δ_m, δ_1, δ_2 are the duty cycles in each sub-intervals. In first sub-interval (0-T/3), the inductor is charged with dc source through switching, the switch S_m for a duty interval of 60% of T/3 while the capacitors C_1 and C_2 are discharging as shown in Fig. 3.

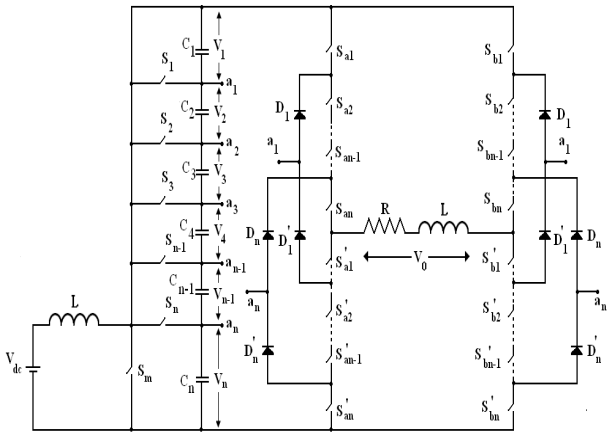


Fig. 1. Generalized multi output dc-dc MLI topology

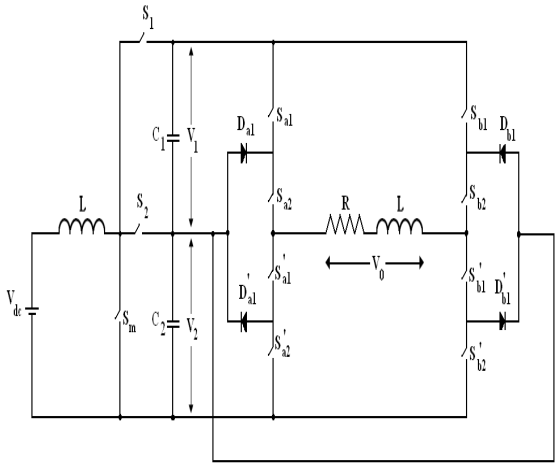


Fig. 2. Power circuit for seven level inverter

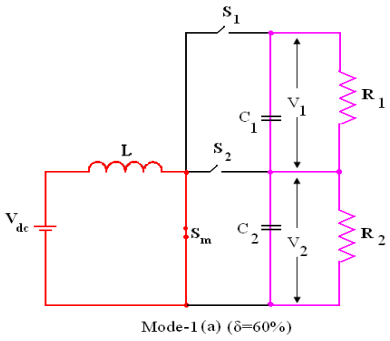


Fig. 3. Operating mode 1 (a)- Inductor charging/ capacitors (C_1, C_2) discharging

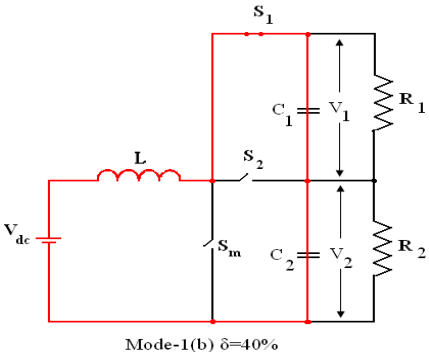


Fig. 4. Operating mode 1 (b)- Inductor discharging and capacitors (C_1, C_2) charging

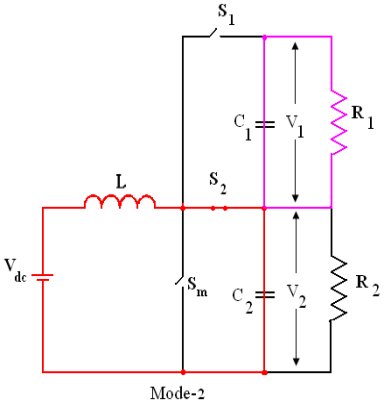


Fig. 6. Operating mode 2- Inductor discharging and capacitor C_1 discharging and capacitor C_2 charging

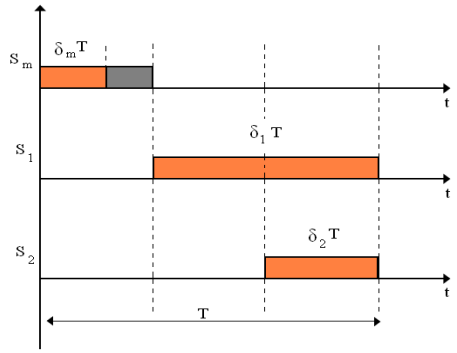


Fig. 7. Timing diagram

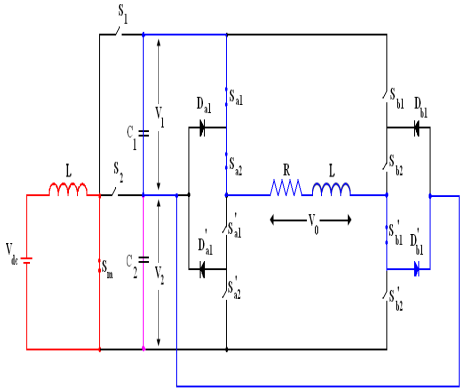


Fig. 8. Mode diagram for synthesizing level V_1

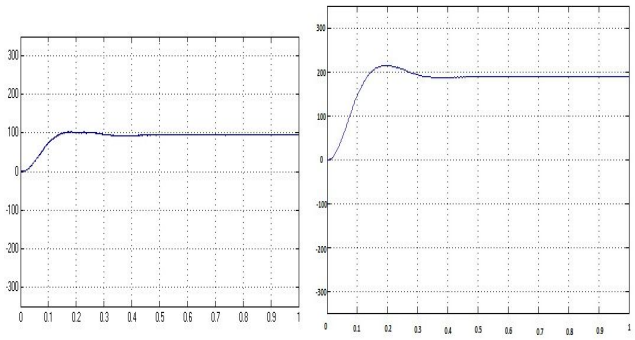
In the same sub-interval shown in Fig. 4, the capacitors get charged through inductor and dc source when the switch S_m is kept open for a duty interval of 40% of T/3. Mode 2 shown in Fig. 5 is initiated between (T/3) and (2T/3) that identical to mode 1 only when S_m is in open condition. Mode 3 seen in Fig. 6 is between (2T/3) and T, the inductor is in discharging mode, capacitor C_1 is discharged and C_2 is charged. Fig. 8 shows the operating mode for extracting the capacitor C_1 voltage to synthesize the voltage level V_1 by switching the switch S_{a1}, S_{a2} and S_{b2}'.

Table 1. Comparison of topologies for 7 level

Multilevel Inverter Structure	Cascaded H-bridge	Diode clamped	Flying capacitor	Proposed Topology
Main switches	12	12	12	10
Bypass diodes	-	-	-	6
Clamping diodes	-	12	-	-
DC split capacitors	-	3	3	2
Clamping capacitors	-	-	12	-
DC sources	3	1	1	1
Total	15	28	28	19

Simulation Results

The proposed topology is simulated for seven level inverter in Matlabr 2010b with simulation parameters: V_{dc}= 100V, R_L=100Ω, L- 106mH, δ_m= 60% (for S_m), $\delta_1 = \delta_2$=20% for (S_1 and S_2) and α_1= 16.58º, α_2= 42.81º, α_3= 68.2º. The main objective is to propose a topology with reduced components and for simplicity, fundamental switching strategy (SHE) is used to test the feasibility of the proposed inverter. The dc-link voltages across capacitors (C_1 and C_2) are shown in Fig. 9. The output voltage waveform for the proposed inverter is shown in Fig. 11.



(a) **(b)**

Fig. 9. Dc-link Voltage across for (a) capacitor (C_1) (b) capacitor (C_2)

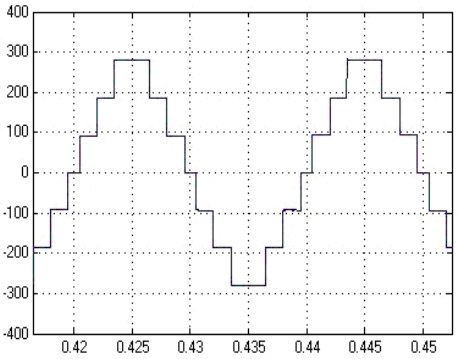


Fig.10. Output voltage waveform

Experimental Results

The experimental setup for the same used in simulation is displayed in Fig.11. The power circuit is constituted by using MOSFETs (IRF 840), clamping diodes (BYQ 28E), capacitors value of 1000uF and inductor (L=100mH). The gating pulse generation methodology is utilized to generate the gating pulses required for the power devices involved in the laboratory prototype (Ramkumar *et al.*, 2012). The gating signals for multi-output dc- dc converter and asymmetrical diode clamped inverters are shown in Fig. 12 and Fig.13. The output voltage waveform is displayed in Fig.14 and its output voltage spectrum. Fig. 15 represents the load current waveform that shows the proposed inverter works well for inductive load.

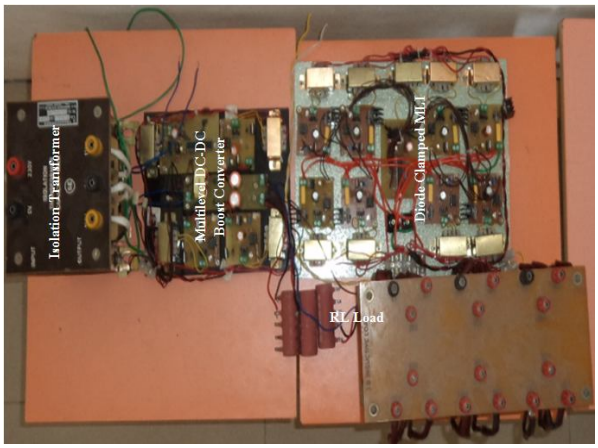


Fig.11. Experimental Setup

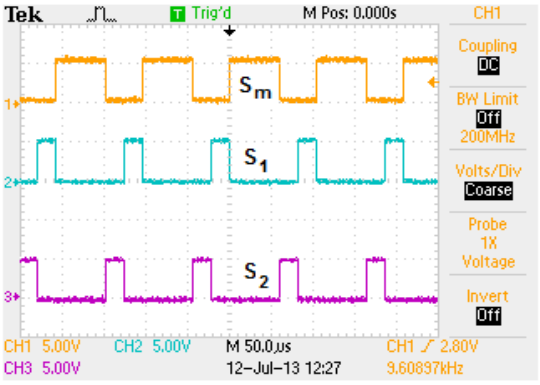


Fig. 12. Gating pulses for multi-output dc-dc converter

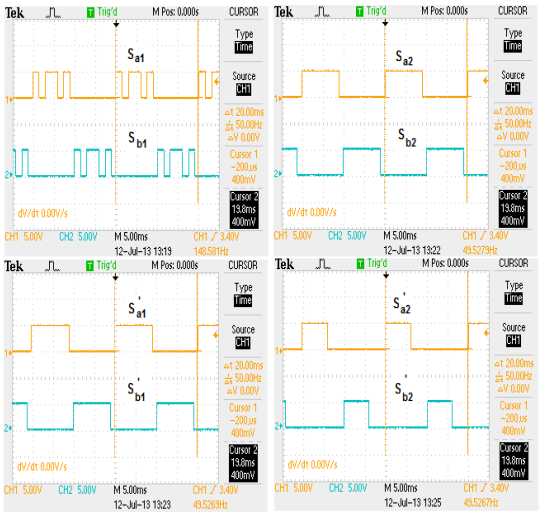
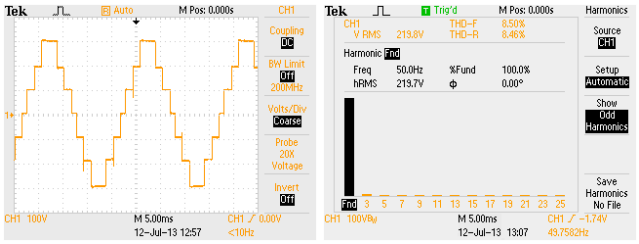


Fig. 13. Gating pulses for diode clamped inverter



(a) **(b)**

Fig. 14. (a) Output voltage waveform (b) Harmonic spectrum

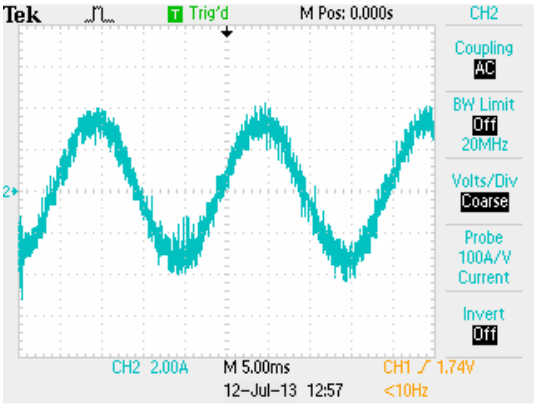


Fig. 15. Load current waveform

Conclusion

A new topology for multi output boost diode clamped inverter is proposed in this paper. Using this circuit, the capacitors are charged with asymmetrical voltages thereby synthesizing the more levels in the load voltage with reduced power components in par with conventional neutral point clamped inverters. This adventure engenders a new avenue to bring various innovations in the multilevel boost inverter family.

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